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MAXIM REPORTS RECORD REVENUES AND EARNINGS FOR THE THIRD QUARTER OF FISCAL 1998

Maxim Integrated Products, Inc., (MXIM) reported record net revenues of $145 million for the third quarter of fiscal 1998 ending March 28, 1998, compared to $111 million for the same quarter in fiscal 1997. Net income increased to $46.1 million in Q398, compared to $35.4 million for the third quarter of fiscal 1997. Diluted income per share was $0.31 per share for Q398, compared to $0.24 per share for the same period a year ago.

During the quarter, cash and short-term investments increased by $57.4 million after purchasing $15.9 million of common stock and $15 million in capital equipment. Net inventory increased by $2.4 million during Q398. Annualized return on average stockholders' equity for the quarter was 32%, one of the highest in the industry today.

Third quarter ending backlog shippable within the next 12 months increased to $216 million from the $208 million reported at the end of Q298. Seventy-three percent of the ending Q398 backlog consists of orders that were requested for shipment in Q498 or earlier.

Net bookings in the third quarter of fiscal 1998 were below the record Q298 level but consistent with our estimates of customer consumption of our products. We believe that customers now perceive that they have sufficient backlog orders placed on Maxim to support their current consumption rates. We also believe that the distribution sales channels overbooked in the first half of 1998, resulting in both reduced bookings and cancellation of approximately $15 million of orders during Q398. Total cancellations for the quarter were $21 million, up from $19 million in Q298.

Gross margins for the third quarter increased to 67.4%, compared to 67% in Q298. Research and development expense increased by $1.7 million, to 12.9% of net revenues. During Q398, the Company also recorded charges of $6 million related to reducing the carrying value of certain pieces of equipment and tooling. In addition, a $5 million increase in inventory reserves further increased cost of sales in Q398.

Jack Gifford, Chairman, President and Chief Executive Officer, commented on the quarter: "We are very encouraged about our new product development activities. During the first three quarters of FY98, we introduced nearly as many new products as we did in all of fiscal 1997. We expect to meet the new product growth objectives that we set for this year."

Mr. Gifford continued: "We believe that the breadth and depth of our proprietary product lines, the acceptance of our new products, and the growth of the emergent markets in which we are investing will support our continued growth through the remainder of fiscal 1998 and beyond."

Safe harbor statement under the Private Securities Litigation Reform Act of 1995: Forward-looking statements in this news release involve risk and uncertainty. There are numerous factors that could cause the Company's actual results to differ materially from results predicted in this news release.

Important factors affecting future revenue growth include whether, and the extent to which, demand for the Company's products increases and reflects real end user demand, whether customer cancellations and delays of outstanding orders increase, and whether the Company is able to manufacture in the correct mix to respond to orders on hand and new orders received in the future.

Semicustom “QuickChip” ASICs implement RF functions to 9GHz

In addition to standard product ICs, Maxim offers a rapid-response ASIC service. Semicustom arrays known as “QuickChips™” provide designers with a selection of uncommitted semiconductor devices: JFETs, Schottky diodes, ESD-protected diodes, MOS capacitors, trimmable nichrome resistors, and bipolar transistors with f_Ts to 27GHz. Completing one of these chips with a custom metal mask set interconnects the selected components to create a high-frequency, high-performance circuit.

A comprehensive set of design, verification, and layout software tools has been developed to ensure a high probability that QuickChip designs will meet their target specifications on the first pass. Both UNIX and PC platforms are supported.

Three different QuickChip families are available. The QC10 family of seven arrays is made with a complementary bipolar process featuring NPN and PNP f_Ts of 9GHz and 6GHz, respectively. It is optimized for analog signal acquisition, amplification, and sourcing.

The QC6 family of four arrays is fabricated in a process with 9GHz NPN and 80MHz PNP f_Ts. These arrays are suitable for a wide range of fiber, IF, and instrumentation applications.

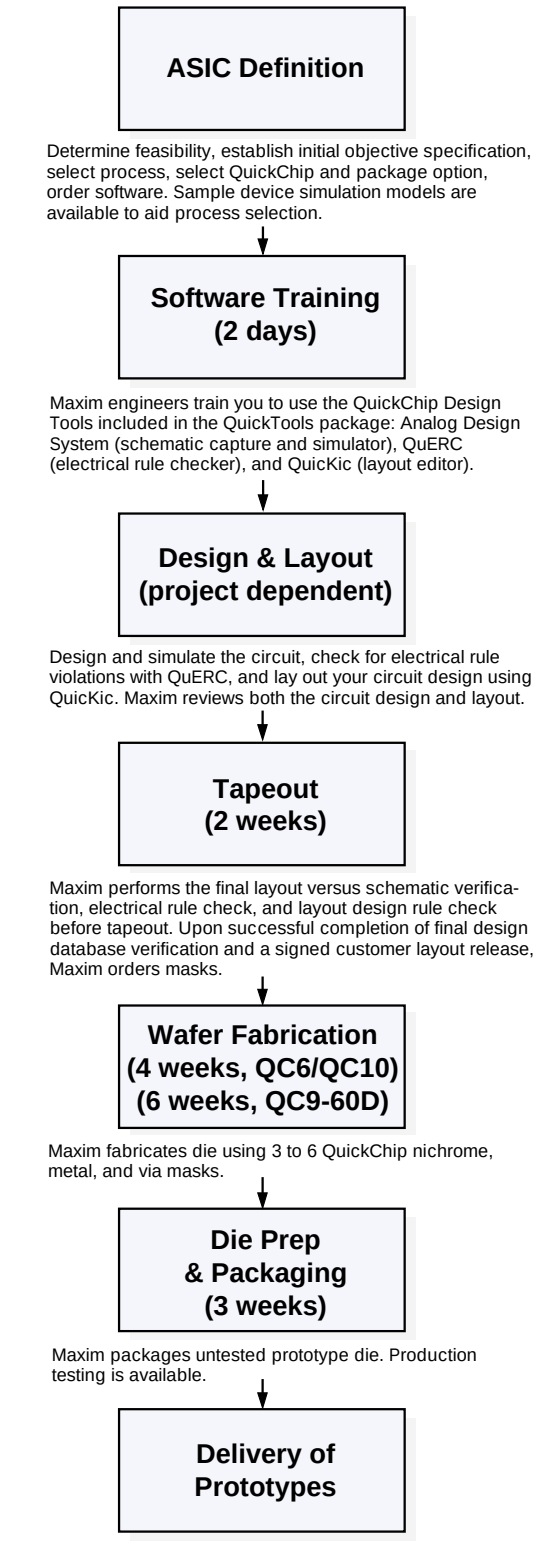
The QC9 array is fabricated in a 27GHz process and is intended for RF and HF applications. More than 35 designs have been completed using the QC9 array since its introduction. These include a 900MHz transceiver, a 7GHz prescaler, several GPS receivers, an OC48 amplifier, pulse and window comparators, and a 2x2 crosspoint switch.

The design examples that follow, reprinted with kind permission of the IEEE, illustrate the capabilities of QuickChip ASICs.

For further information, or to request a copy of Maxim’s *High-Frequency ASIC Development Handbook*, contact Maxim’s HF ASIC Group, attention Raj Garg, via FAX at 503-644-9929.

QuickChip is a trademark of Maxim Integrated Products.

Maxim’s QuickChip IC Design Approach



QuickChip Design Example 1

A Silicon Bipolar Broadband PLL Building Block Integrated Circuit

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Abstract:

A broadband phase-lock loop building block IC that can accommodate signal frequencies from 0.5GHz to 9GHz is presented. The design integrates a prescaler with selectable divide ratio, a phase detector, a voltage-controlled oscillator for production testing, and associated circuitry. The chip is designed in a silicon bipolar linear array technology and packaged in a 16-pin plastic dual in-line package. The result is a low-cost, broadband solution for a variety of PLL systems.

Introduction:

The development focus for many high-speed PLL designs is evolving from research to economic challenges. System designers are calling for highly integrated, price-competitive solutions. A low-cost solution often requires the use of an inexpensive plastic package despite its detrimental effect on high-speed performance. A higher level of integration results in greater power dissipation, further increasing the challenges associated with a plastic package. Thus, the goal of the PLL building block described in this paper was to achieve broadband performance with low power dissipation and have the performance minimally affected by package limitations.

Design:

The PLL building block IC can accommodate an input signal frequency range from 0.5GHz to 9GHz making it effective for most PLL applications such as satellite communication systems, high-speed measuring equipment, and RF data communications. The chip was fabricated in a silicon bipolar technology, with NPN transistor f_T and f_{max} equal to 24GHz and 22GHz, respectively. To improve the time-to-market, a linear array was used. The linear array is analogous to a gate array except that, instead of having pre-placed gates for digital functions, the linear array has pre-placed elements such as transistors, resistors, and capacitors for analog designs. A faster turnaround time may be achieved using a linear array, but increased layout parasitics and a fixed number of elements and element values can prevent the designer from achieving an optimum design. Despite these potential limitations, broadband performance was still achieved through careful layout and creative designs, which used the available components most effectively.

A block diagram of the chip is shown in Figure 1. The chip receives a modulated signal from an external source within the 0.5GHz to 9GHz frequency range. The signal is phase-locked to an external RF input with an on-chip phase detector and off-chip loop filter. The prescaler is divided into two sections: a divide-by-eight block and a divide-by-eight/nine block. The VCO, charge pump, and loop filter were left off-chip so that the building block could be used in a variety of system applications.

The flip-flops in the divide-by-eight use a master/slave configuration with the Q-bar output fed back to the data input to divide the clock frequency by a factor of two. A schematic of the first flip-flop in the divide-by-eight

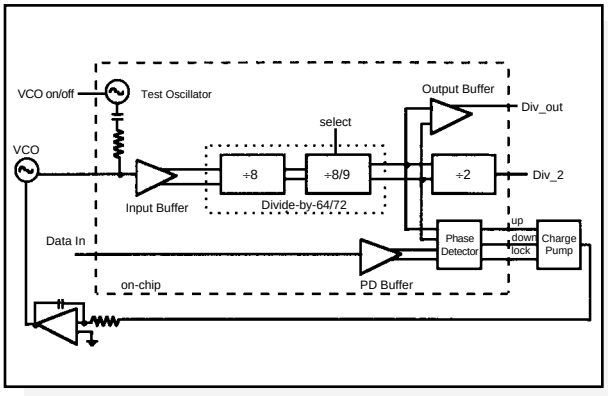

Figure 1. PLL Building Block and complete PLL circuitry

chain is shown in Figure 2. A special feature of the first flip-flop is the inclusion of currents referred to as "keep-alive" currents and denoted I_K in the schematic. Keep-alive currents reduce the time to fully switch Q_9 - Q_{16} by keeping the transistors from turning off. Values on the order of 1/10 the main differential-pair current (I_D) were used. All eight emitter-followers (Q_1 - Q_8) were necessary for the first flip-flop in the divide-by-eight since the low output impedance and high current-drive capability of the emitter-followers increase the toggle rate. For following stages when speed was not a concern, the emitter-followers were eliminated (or reduced in number) and the differential-pair currents were reduced to minimize power dissipation.

The phase detector in this work is based on a standard design. A block diagram of the phase detector is shown in Figure 3. There are three outputs of the phase detector: UP, DWN, and LD. When the loop is out of lock, an irregular pulse train appears on either the UP or DWN outputs depending on whether the input signal frequency is faster or slower than the reference frequency. The filtered output of the other signal remains high. If the signal frequency and reference frequency are equal, the output pulse train is periodic and the average value a measure of the phase offset.

The development of low-cost "at-speed" testing of the PLL building block is key to its success in production. An on-chip, high-frequency (~ 5GHz) ring oscillator is included. The purpose of the oscillator is to provide a method to test the frequency dividers during near-speed wafer or package testing. The VCO is a ring oscillator that uses interpolation to increase the frequency response [1]. The oscillator is powered separately through an external "enable" pin that disables its operation when grounded and allows operation when tied to the supply. The divide-by-two circuitry is used to reduce the test output signal to a frequency compatible with low-speed wafer testing and die-sorting.

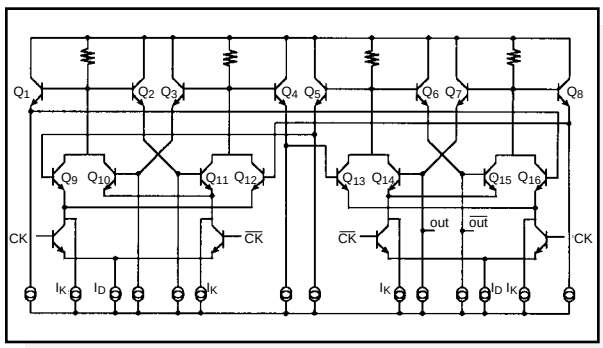

Figure 2. Schematic of first flip-flop in divide-by-eight chain.

Packaging:

Successful operation of the PLL building block IC at high-frequencies required careful re-design of the plastic package as shown in Figure 4. Ground inductance was required to be absolutely minimized to achieve good phase noise response. The high-frequency prescaler input (VRF) was required to be well isolated from the phase detector input (REFIN). Six of the 16 pins on the SOIC package are ground pins and they are shorted to the paddle. The retooling provides a relatively "clean" ground point for the chip grounds and chip substrate to be connected. Surrounding the high frequency input signal with four of the ground pins (two on each side) improved the isolation of the input signal. Furthermore, retooling the package helped significantly improve the thermal

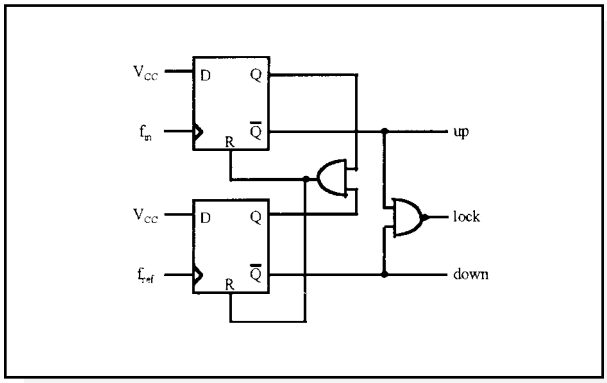

Figure 3. Phase Detector Block Diagram

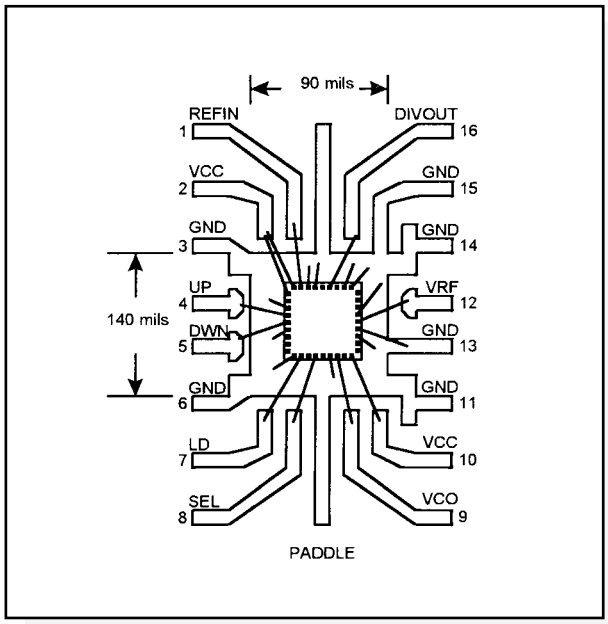

Figure 4. Package Drawing

resistance. The Φja of the package was reduced from ~100°C/W to 72°C/W and the maximum junction temperature of the chip under all cases never exceeds 125°C.

Based on the physical characteristics of the package, a lumped parameter package model was developed. Figure 5 shows the model, with specific parameter values that were used for simulation. (The values given are for the shortest lead lengths.) The high-frequency input signal was placed in the center of the package to minimize bond wire and lead inductance, resulting in lower coupling and improved matching.

Measured Results:

The minimum detectable input signal versus input frequency for the packaged PLL building block is shown in Figure 6. An input signal of -20dBm or less is sufficient for operation over a broad range of frequencies. The design functions from 0.5GHz to 9GHz but requires slightly larger input power levels at the frequency bounds. Measurements of the packaged die were taken over a range of temperatures (-35°C to +90°C). At lower temperatures, the PLL building block functions at higher speeds for a given input signal level because the transistor f_T increases for decreasing junction temperatures. Simulation results predict the effects of temperature on performance. At each temperature the supply was varied from 4.5V to 5.5V. The data in Figure 6 shows that the performance of the circuit is relatively independent of supply voltage.

Divider sensitivity was also measured for the unpackaged die using a membrane probe. The similarity of the two curves shown in Figure 7 demonstrates the broadband performance of the package. There is little difference between wafer and package measurements up to 9GHz.

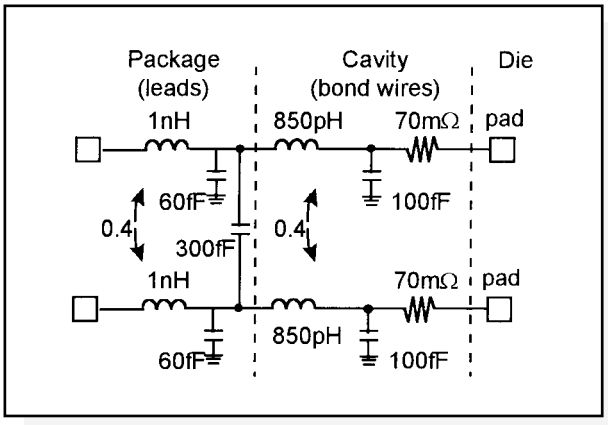

Figure 5. Package Model

The input buffer driving the divider is designed to match to a 50Ω impedance. The measured results of S_{11} shown in Figure 8 can be explained with an understanding of the input buffer topology. The impedance match is

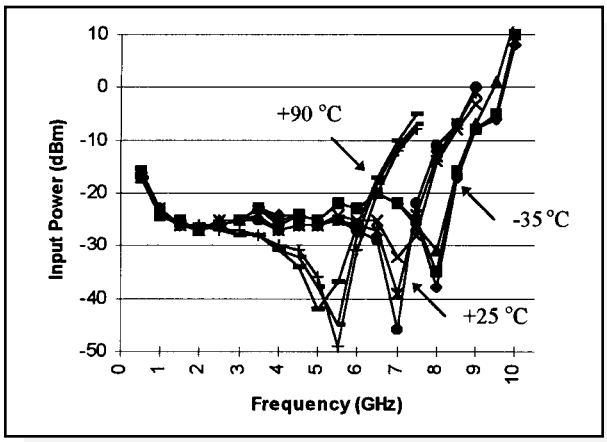

Figure 6. Divider Sensitivity of packaged devices over various supply voltages and temperatures.

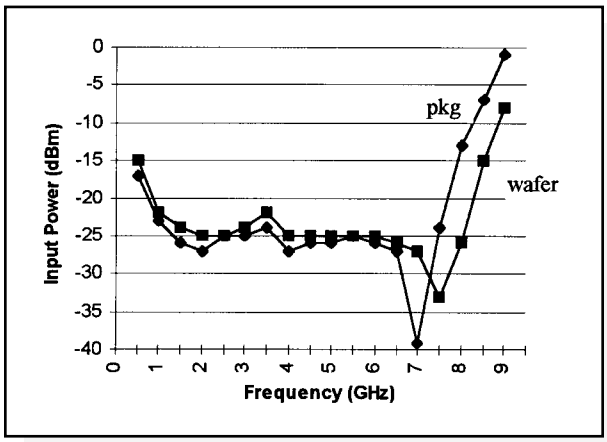

Figure 7. Divider Sensitivity: comparison of package and wafer probe data under nominal conditions. (T = 25°C, V_{CC} = 5V)

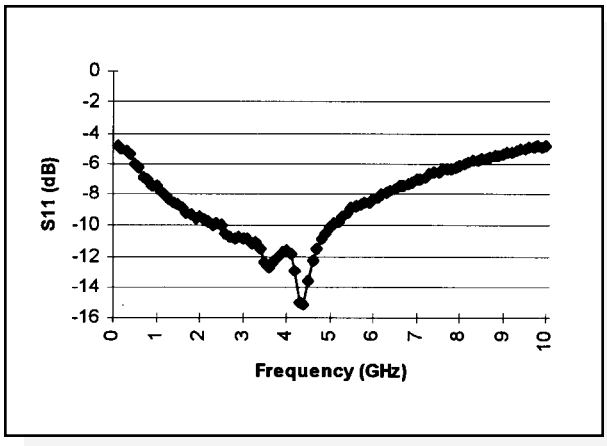

Figure 8. Input impedance of packaged PLL building block.

achieved through a 50Ω internal resistor connected between the input and a bias voltage. At very low frequencies, the impedance of the bias circuitry increases the input impedance. Capacitance at the bias node lowers the impedance of the bias circuitry as the frequency increases. A good match is achieved mid-band. At high frequencies, package and layout parasitics begin to degrade the input impedance. The data shown also reflects the impedance of an SMA connector which further degrades performance at high frequencies. Better than -5dB for S_{11} can be achieved over the full band of operating frequencies which is adequate for most closed-loop applications.

The oscillation frequency of the on-chip oscillator used for test purposes is approximately 5GHz. The design was not optimized for speed and higher frequencies can be achieved with this design. The measured phase noise is -69dBc/Hz at an offset frequency of 100kHz.

The phase detector functions properly over the entire range of the divider. The outputs are open collector with external loading. With 150Ω loads, the output voltage on the UP and DWN pins is 1.1V. The LD output achieves a 2V swing when loaded with a 500Ω resistor. The minimum reference input signal required is -18dBm (matched to 50Ω) and can tolerate as much as +10dBm.

The circuit die size is 70 mil x 75 mil. Roughly 85% of the linear array was utilized for the design of the PLL building block. Power dissipation under nominal conditions (T = 25°C and V_{CC} = 5V) is approximately 500mW.

Conclusions:

The design described in this paper is a broadband PLL building block capable of accommodating signal frequencies ranging from 0.5GHz to 9GHz. The manufactured part exemplifies a low-cost, fast time-to-market, design without sacrificing performance. This chip overcomes design problems associated with inexpensive packaging through effective package modeling, built-in testing, and retooling.

Acknowledgment:

The authors wish to thank Larry Blue, Tom Jackson, and Steve Rosenbaum from Hughes Network Systems and Will Grimes from Maxim Integrated Products for their help in the development of the PLL Building Block.

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QuickChip Design Example 2

Low Power Silicon BJT LNA for 1.9GHz

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Abstract

A two-stage 1.9GHz monolithic low-noise amplifier (LNA) with a measured noise figure of 2.3dB and an associated gain of 15dB was fabricated in a standard silicon bipolar transistor array. It dissipates 5.2mW from a 3V supply including the bias circuitry. Input return loss and isolation are -9dB and -20dB, respectively.

I. Introduction

In portable communication equipment, such as cellular phones and digital cordless phones, manufacturers are trying to replace as many discrete devices as possible with high-density ICs to be competitive in size, weight, power dissipation, and price. In a number of recent papers low power LNAs for S-band have been described [1,2,3]. These LNAs were fabricated using some sophisticated GaAs full-custom processes. Since the high frequency performance of state-of-the-art silicon bipolar processes are continuously improving lowcost semi-custom arrays with a limited choice of components provide a reasonable solution for RF applications.

In order to demonstrate such a solution, we present in this letter a very low-power monolithic 1.9GHz silicon LNA which draws a total current of 1.75mA including bias circuit.

II. Circuit Design

A schematic of the two-stage LNA is shown in Fig. 1. The circuit employs a high-gain common-emitter stage (Q1-RL) and a emitter-follower output stage (Q2-Q3). This approach eliminates the need for coupling capacitors. The current of the first stage is set by a resistive parallel feedback (R3 and R4), which is connected to the external matching inductor (L1) such that no noise degradation occurs. Thus, only a single supply voltage is required. This feedback also improves both the bias and RF stability of the amplifier.

The circuit was simulated with Spice and with a linear simulator based on measured S- and noise parameter data of the active device. Good agreement between simulated and measured performance is found as shown in Fig. 2.

III. Measurements

The circuit was fabricated on a 'Quickchip' transistor array with the Maxim GST-2 foundry process. Fig. 3 shows the gain and noise figure of the circuit measured with the HP8970B/HP8971C noise figure meter. The

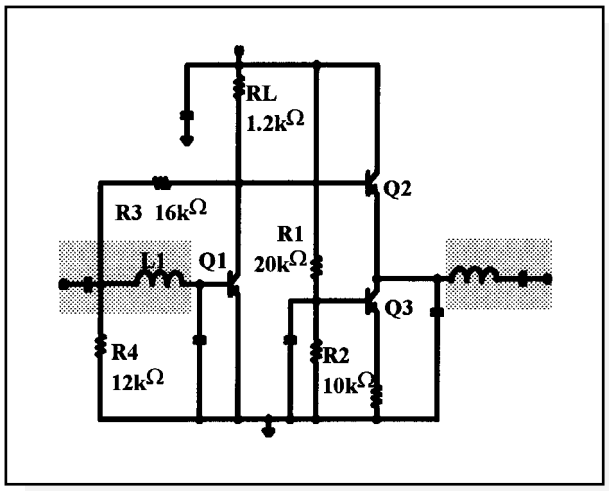

Figure 1. Simplified schematic of the LNA (gray area: off-chip matching)

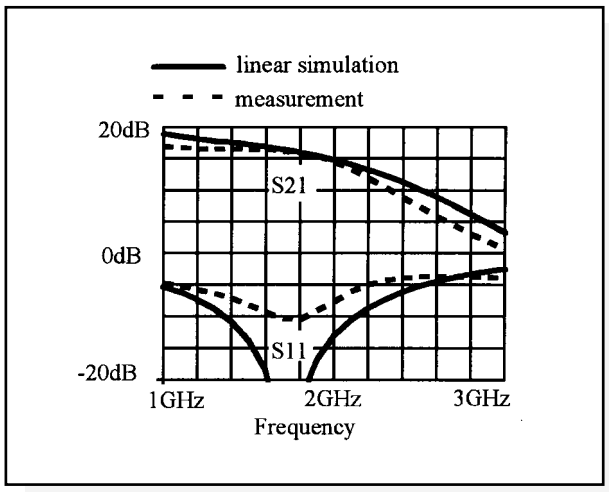

Figure 2. Simulated vs. measured gain and input return loss

amplifier shows a rather flat frequency response of the noise figure from 700MHz up to 2GHz. The best 50Ω noise figure of 2.3dB is achieved between 1.7 and 2.3 GHz. Note that the active device has a minimum noise figure of 1.5dB at 1.9GHz.

The small signal gain is larger than 15dB up to 2GHz at the nominal bias of 3V. The corresponding gain/DC-power figure of merit is 2.9dB/mW. Compared to other L-band LNAs, this design shows low power consumption and a competitive noise figure as seen from Fig. 4.

The noise figure is also quite insensitive to bias voltage variations. Varying the supply voltage from 2.7 to 5V the noise figure remains between 2.2 and 2.5dB.

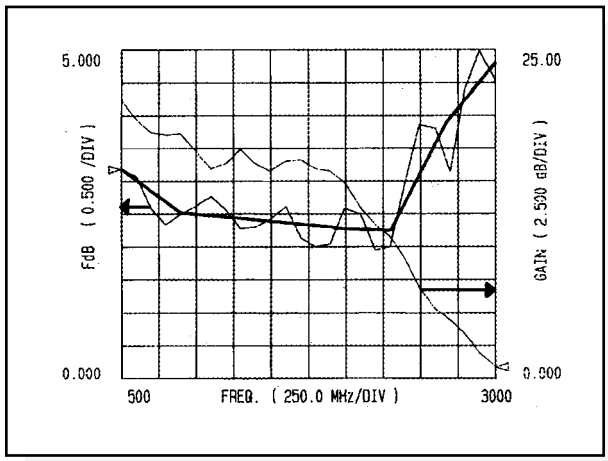

Figure 3. Measured gain and noise figure (V_{CC} = 3V, I_{CC} = 1.75mA (bold line: average noise figure)

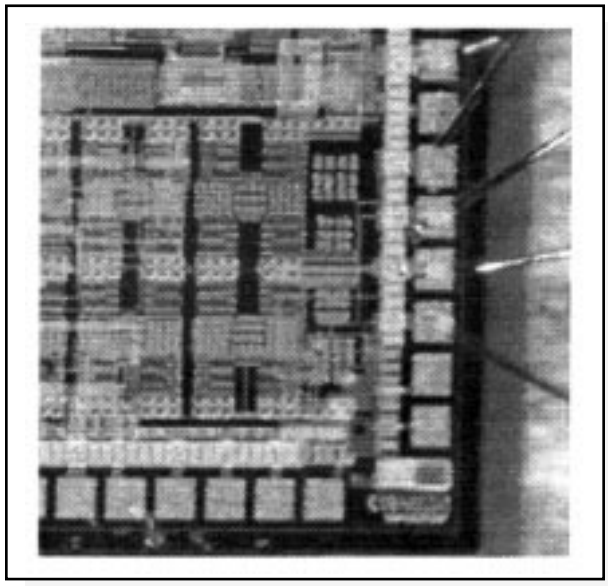

Figure 5. shows a photograph of the lower right part of the 1.9 x 1.8 mm² large chip containing the LNA. In Fig. 6 the chip can be seen as mounted on the substrate and bonded to the printed input and output matching inductors.

The designed amplifier has a measured -1dB input compression point of -24dBm, which equals an output compression point of -9dBm. The third order intermodulation intercept point is measured at -21dBm input power. This is adequate for DECT handheld terminal.

Fig. 5 shows a photograph of the lower right part of the 1.9 x 1.8mm² large chip containing the LNA. In Fig. 6 the chip can be seen as mounted on the substrate and bonded to the printed input and output matching inductors.

IV Conclusions

A silicon bipolar low power LNA for 1.9GHz has been designed and tested. It shows a noise figure of 2.3dB

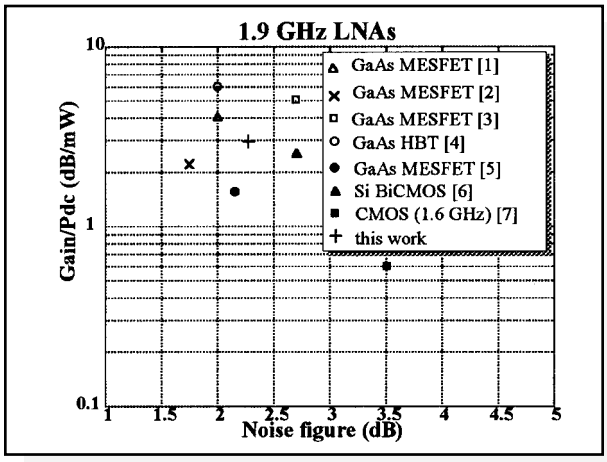

Figure 4. Gain to DC power ratio plotted versus noise figure for several state-of-the-art L- and S-band LNAs

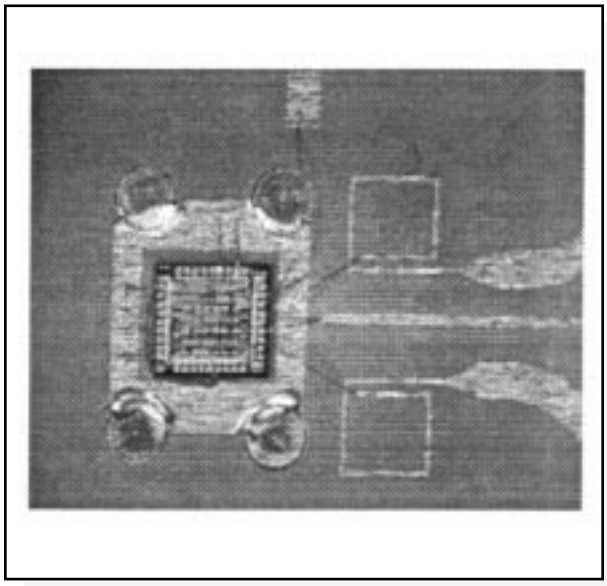

Figure 6. Photograph of the Quickchip mounted on the test substrate. On the right are the printed inductors for input and output matching.

along with a 15dB gain. The power consumption is only 5.2mW resulting in a high gain/DC-power figure of merit of 2.9dB/mW. The design was done on a transistor array showing almost no performance degradation relative to full custom design.

V Acknowledgement

The authors wish to acknowledge MAXIM for providing access to their GST-2 Quickchip technology.

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Serial-control multiplexer expands SPI chip selects

SPI™ and Microwire™ buses offer a popular and convenient means for minimizing the number of wires required in connecting smart peripherals to a microcontroller (µC). These synchronous buses comprise a serial-clock, data-in, and data-out line in addition to a chip-select line for each peripheral.

A scheme of one chip-select line per device, however, can quickly use up the precious port pins in a µC system. To mitigate this situation, the dual 4-channel analog multiplexer in **Figure 1** (an SPI device itself) multiplexes a single port pin (PC0) to provide chip selects for four other SPI peripherals in the system. A second port pin (PC1) selects the multiplexer.

All switches in this multiplexer are bidirectional. Its two sections are independent, and either output (unlike those of conventional differential multiplexers) can be programmed to connect to any, all, or none of its four input channels. Thus, the second (top) section is employed, independently of the lower section, to expand the number of analog channels available to the µC. The µC's internal multiplexer supports 8 channels, so this scheme (using one to get four more) yields a total of 11 input channels.

SPI is a trademark of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

By operating "backwards," the lower 4:1 mux routes the PC0 signal to the $\overline{CS}$ input of a selected peripheral. Driving PC0 low selects that peripheral for receiving SPI data, and driving PC0 high deselects all four peripherals. Read and write sequences are the same as in regular SPI systems, except the chip selects must be set up beforehand. PC0 then goes low, the read/write operation is executed, and PC0 returns high to deselect the device.

This procedure is not burdensome in practice. Typical SPI systems include a device that is serviced often (such as a display driver), and several others that require service only occasionally (such as EEPROMs or real-time clocks). Thus, the chip-select mux can leave the heavily used device selected most of the time, and perform an update only when selecting a new device.

To accommodate other combinations of chip-select and analog-expansion lines, replace the MAX350 with a similar device such as the MAX395, whose eight serially addressed SPST switches can be configured as required.

A similar idea appeared in the 3/23/98 issue of Electronic Design.

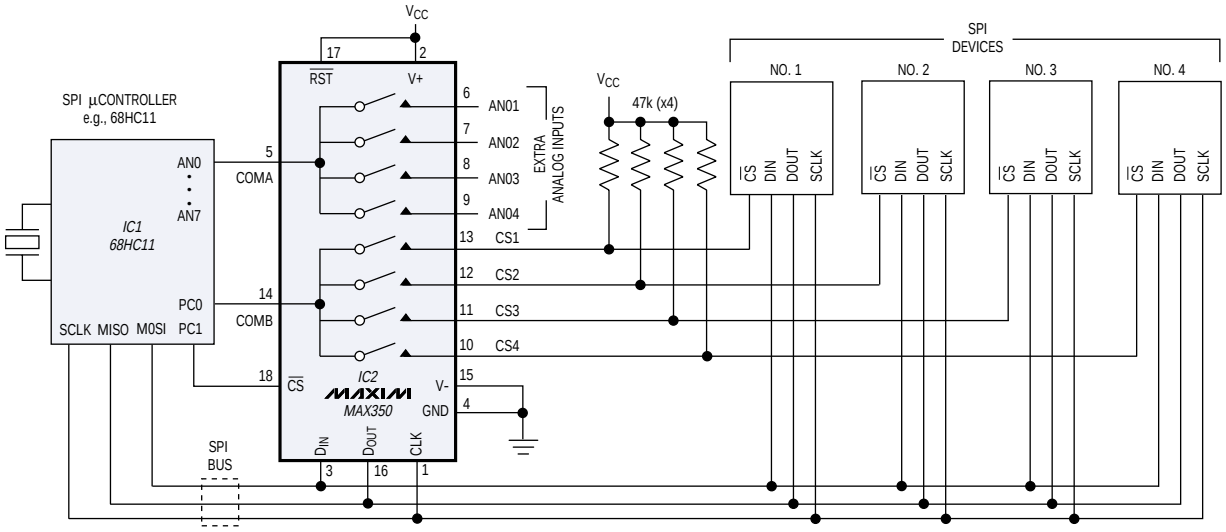


Figure 1. A dual 4-channel multiplexer expands the number of input channels and chip-select lines this microcontroller can support.

Circuit connection adds current-mode operation to PFM boost converters

A control scheme used in certain boost-controller ICs from Maxim (current-limited pulse-frequency modulation, or PFM), achieves high efficiency over a wide range of output current by combining the low quiescent current of PFM with the load-driving capability of pulse-width modulation (PWM). To provide current-mode control as well, simply connect the load, output filter capacitor, and lower feedback resistor to the current-sense pin (CS) instead of ground **(Figure 1)**.

When operating with medium to heavy loads, the Figure 1 circuit exhibits lower output ripple and a more stable inductor current **(Figure 2a)** than do the standard application circuits represented by typical waveforms in **Figure 2b**. The improvements gained by these connections have no effect on the quiescent current and require no additional circuitry, but they do require separate input and output grounds as shown, connected only by R_{SENSE}.

This circuit achieves current-mode control by constantly monitoring the inductor current through R_{SENSE}: via the field-effect transistor during t_{ON} (which depends on the magnitude of V_{IN}), and via the diode and output filter capacitor during t_{OFF} (minimum 2.3µs). Flowing through R_{SENSE}, the inductor current creates a signal at CS that couples through the output filter capacitor and adds to the normal feedback signal at FB. Connecting the load between OUT and CS prevents this CS signal from adding to the ripple at V_{OUT}.

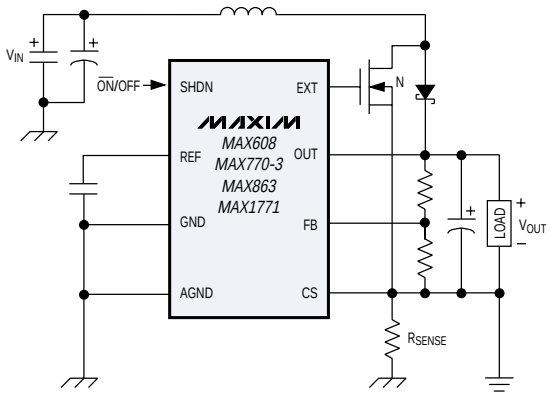
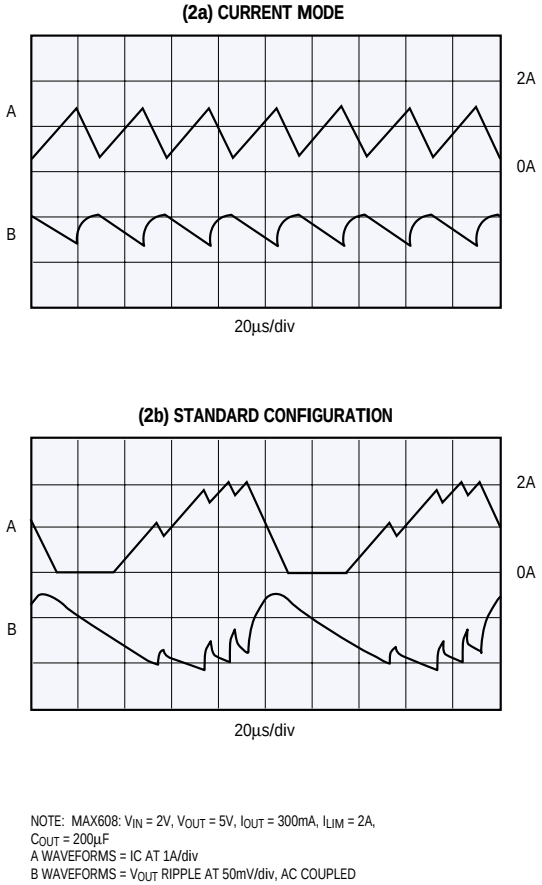


Figure 1. This circuit adds current-mode operation to Maxim's current-limited PFM boost controllers without increasing the quiescent current.



NOTE: MAX608: V_{IN} = 2V, V_{OUT} = 5V, I_{OUT} = 300mA, I_{LIM} = 2A, C_{OUT} = 200µF
A WAVEFORMS = IC AT 1A/div
B WAVEFORMS = V_{OUT} RIPPLE AT 50mV/div, AC COUPLED

Figure 2. The Figure 1 circuit's inductor-current and output-ripple waveforms (a) exhibit better stability and lower ripple amplitude than those of the standard operating configuration (b).

Voltage-inverter IC forms high-efficiency rail splitter

A switched-capacitor voltage inverter configured as a "rail splitter" (IC1 in **Figure 1**) provides a bipolar (dual-rail) local power supply that is useful in single-rail systems featuring one or more dual-rail ICs. Moreover, the tiny SOT-23 package and associated components require very little board area.

After power is applied, the flying capacitor (C2) connects alternately across the storage capacitors C3/C4 and C5/C6. This action equalizes the voltages on those capacitors and draws current from V_{IN} or V_{OUT} as required to maintain $V_{OUT} \approx {}^1/_2V_{IN}$.

If the loads across V_{IN}-V_{OUT} and V_{OUT}-0V are equal, the IC sits in a quiescent state and draws about 36µA. To keep V_{OUT} at the mid-rail level, the flying capacitor needs only to supply the difference current caused by unbalanced loads. Efficiency is degraded by the IC's quiescent current for load currents below 100µA, but above 1mA the efficiency is greater than 90%—an excellent feature for low-power or battery-powered applications. (Voltage error and efficiency vary with the load current, as shown in **Figures 2** and **3**.)

This switched-capacitor circuit provides better regulation than that of a simple voltage divider, and better efficiency than that of a simple combination of divider and op-amp buffer. Its main drawback is the increase in output noise with load (see **Table 1**). V_{IN} is restricted (by the IC specifications) to a maximum of 5.5V, which is the maximum voltage allowed between pins 2 and 4 or between pins 1 and 4.

A similar idea appeared in the 8/1/97 issue of EDN.

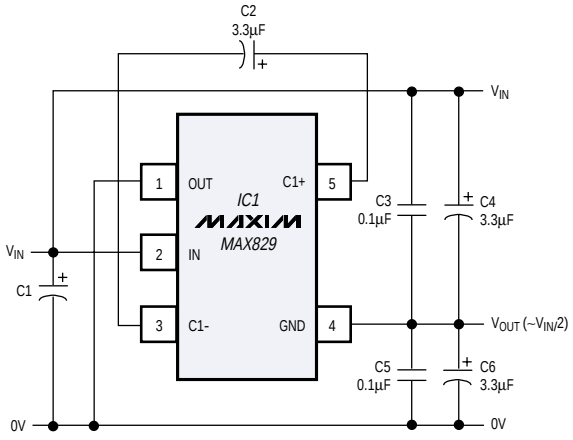


Figure 1. This compact and efficient charge-pump circuit implements a local dual-rail supply for single-rail systems.

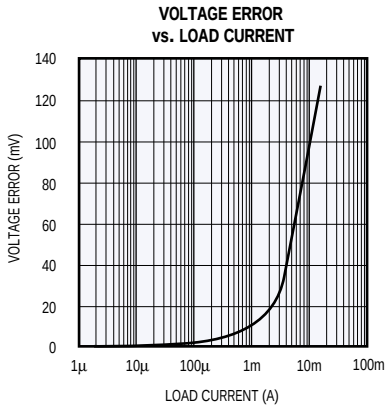


Figure 2. The output voltage error in Figure 1 increases with load current.

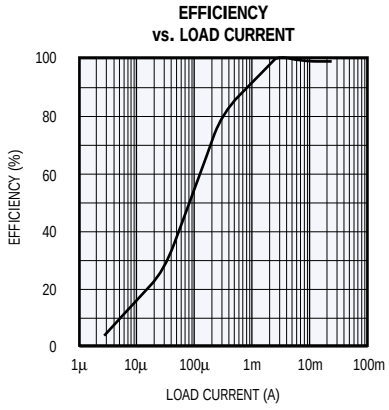


Figure 3. Efficiency also increases with load current in Figure 1.

Table 1. Rail-Splitter Performance (V_{IN} = 5V)

R_{LOAD} (Ω)	INPUT CURRENT (µA)	V_{OUT} ERROR (mV)	OUTPUT CURRENT (µA)	RIPPLE (mVp-p)	EFFICIENCY (%)
∞	36.5	—	—	—	—
10M	36.5	—	0.25	—	0.34
1M	37.7	—	2.5	—	3.32
100k	48.9	0.1	25	—	25.56
10k	156	1.4	250	~1	80.04
1k	1240	13.5	2490	~5	99.72
470	2630	28.5	5260	~8	98.83
100	11,410	126.9	23,700	~30	98.71

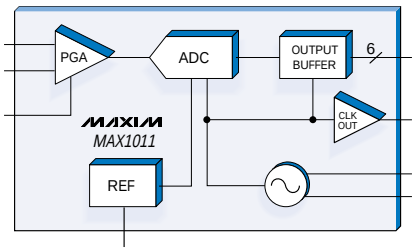
NEW PRODUCTS

Low-power, 6-bit ADC offers sampling rates to 90Msps

The MAX1011 A/D converter combines low power (190mW) and high speed (sampling rate up to 90Msps) with an internal reference and a clock oscillator with overdrive capability. Its ability to convert baseband signals directly makes the MAX1011 suitable for use in IF sampling receivers, VSAT receivers, and QAM demodulators.

The input amplifier's -0.5dB analog bandwidth is 55MHz, and its true differential inputs have user-selectable, full-scale ranges of 125mVp-p, 250mVp-p, and 500mVp-p. The input offset for AC-coupled signals is typically less than ±1/4LSB. Integral and differential nonlinearity (INL and DNL) are also typically less than ±1/4LSB. The effective number of bits is 5.85LSB for 20MHz input signals and 5.7LSB for 50MHz signals.

The MAX1011 operates with a +5V analog supply and a +3.3V digital supply. Available in a 24-pin QSOP, it costs $2.95 (1000 up, FOB USA).



Signal conditioner for piezoresistive sensors is accurate to within 0.1%

The MAX1457 is a monolithic analog-signal processor optimized for the calibration and compensation of piezoresistive sensors. Included are a programmable current source for sensor excitation, 3-bit programmable-gain amplifier (PGA), 12-bit A/D converter, uncommitted op amp, and five 16-bit D/A converters. By compensating the sensor for offset, full-span output (FSO), offset temperature coefficient (TC), FSO TC, and full-span output nonlinearity, the MAX1457 achieves a total error rate less than 0.1% of the sensor's repeatability error.

D/A converters enable the MAX1457 to compensate 1st-order temperature error by adjusting the sensor's span and offset. If necessary, higher order residual errors can then be compensated using interpolation of 1st-order coefficients stored in an external EEPROM look-up table.

The MAX1457 combines three traditional sensor-manufacturing operations: pretest, in which a test computer acquires the sensor-performance data; calibration and compensation, in which coefficients determined from the pretest data are stored in an external EEPROM; and final test, in which the calibration and compensation are verified without removing the transducer from its pretest socket.

An internal, uncommitted op amp can be used to increase the circuit gain or help implement a 2-wire, 4-to-20mA current-transmitter output. The MAX1457 serial interface, compatible with Microwire™ and SPI™ standards, connects directly to an external EEPROM. And by enabling the manufacture and calibration of multiple sensor modules, the MAX1457's built-in test capability lowers manufacturing costs. The MAX1457 is optimized for use with piezoresistive sensors, but a few additional external components enable it to operate with accelerometers, strain gauges, and other resistive sensor types.

The MAX1457 is available in 32-pin TQFP and 28-pin wide SO packages, with prices starting at $9.95 (1000 up, FOB USA). An evaluation kit is available and recommended for proper analysis of the device.

Microwire is a trademark of National Semiconductor Corp.

SPI is a trademark of Motorola, Inc.

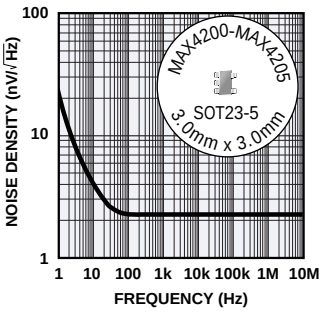
Ultra-high-speed SOT23 open-loop buffers offer low power, low noise

The MAX4200–MAX4205 series of ultra-high-speed open-loop buffers have a proprietary architecture that enables high-speed performance: the MAX4201/MAX4202 devices offer -3dB bandwidths of 780MHz and 0.1dB gain flatness to 280MHz, and all offer 4200V/µs slew rates. Operating from ±5V supplies and drawing quiescent currents of only 2.2mA per buffer, they offer an excellent driving capability for capacitive loads. MAX4200/MAX4203 outputs can drive a minimum of ±90mA.

These single (MAX4200–MAX4202) and dual (MAX4203–MAX4205) buffers differ in their internal back-termination resistor values: 50Ω for 50Ω transmission lines (MAX4201/MAX4204) and 75Ω for 75Ω transmission lines (MAX4202/MAX4205). The MAX4200 and MAX4203 have no internal termination resistors.

High speed and low noise (2.1nV/√Hz voltage-noise density and 0.8pA/√Hz current-noise density) suit these buffers for use in data communications and in driving the inputs of high-speed A/D converters. Single buffers come in 5-pin SOT23 and 8-pin SO packages; duals come in 8-pin µMAX and SO packages. Prices start at $1.70 (1000 up, FOB USA).

INPUT VOLTAGE NOISE DENSITY



NEW PRODUCTS

SOT23, ultra-low-voltage, beyond-the-rails op amps draw only 10µA

The MAX4240–MAX4244 series of single/dual/quad, low-power, low-voltage op amps feature Beyond-the-Rails™ inputs and Rail-to-Rail® outputs that allow the full range of supply voltage to be used for signal range. The op amps provide 90kHz gain-bandwidth products while drawing only 10µA per amplifier. In portable and battery-powered systems, two AA alkaline cells enable operation up to 200,000 hours.

MAX4240–MAX4244 op amps operate from a single supply of +1.8V to +5.5V or a dual supply of ±0.9V to ±2.75V. The MAX4241 and MAX4243 have a shutdown mode that places the outputs in a high-impedance state and lowers the supply current to only 1µA. The input common-mode range extends 200mV beyond each rail, and with 100kΩ loads the outputs typically swing to within 8mV of each rail. The op amps feature 200µV input-offset voltages and outputs that are unity-gain stable for capacitive loads to 200pF.

Package options are a tiny SOT23-5 (the single MAX4240), an 8-pin µMAX (the single MAX4241), an 8-pin µMAX or SO (the dual MAX4242), a 10-pin µMAX or 14-pin SO (the dual MAX4243), and a 14-pin SO (the quad MAX4244). Prices start at $0.83 (1000 up, FOB USA).

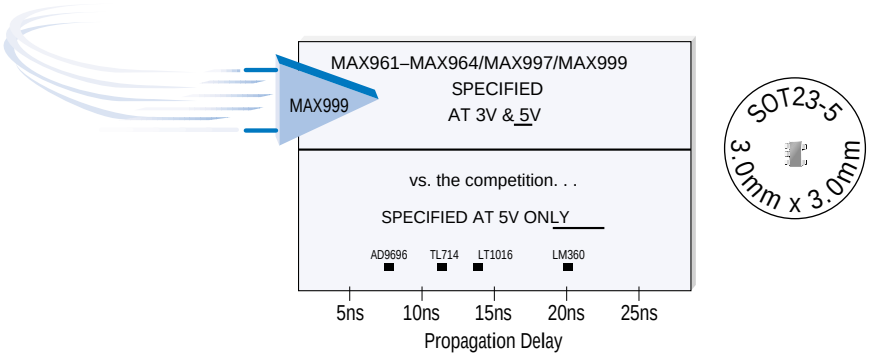
Beyond-the-Rails is a trademark of Maxim Integrated Products.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Low-power, single-supply comparators deliver 4.5ns propagation delays

The MAX961–MAX964 and MAX997/MAX999 are low-power, ultra-high-speed single/dual/quad comparators. Featuring 4.5ns propagation delays with 5mV overdrive, they each include 3.5mV of internal hysteresis and draw quiescent supply currents of only 5mA per comparator. All are optimized for both 3V and 5V single-supply operation. Input common-mode ranges extend 100mV beyond-the-rails, and the outputs can sink or source 4mA to within 0.52V of ground or V_{CC}.

All but the MAX962 and MAX999 have a shutdown mode that lowers the supply current to 270µA per comparator, and the MAX961/MAX963 have complementary outputs with a latch-enable that allows the user to hold valid output states. Package options include a space-saving 5-pin SOT23 for the single MAX999, an 8-pin SO or µMAX for the single MAX961/MAX997 and dual MAX962, a 14-pin SO for the dual MAX963, and a 16-pin narrow SO or QSOP for the quad MAX964. Prices start at $1.97 (1000 up, FOB USA).

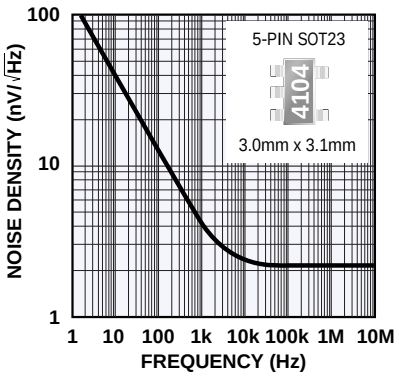


Low-noise, low-distortion op amps deliver 880MHz in SOT23-5 package

The MAX4104/MAX4105 and MAX4304/MAX4305 ultra-high-speed, low-noise op amps offer wide output swings (±3.4V with 100Ω load) and high output-current capability (±70mA). Their low input noise-voltage density (2.1nV/√Hz) and spurious-free dynamic range (-88dBc) make them ideal for low-noise, low-distortion applications in video and telecommunications.

The MAX4104 is unity-gain stable and draws only 20mA while delivering 880MHz bandwidths and 400V/µs slew rates. The MAX4304, compensated for a minimum gain of 2V/V, delivers 730MHz and 1000V/µs. The MAX4105 is compensated for a gain of 5V/V or greater, and delivers 430MHz and 1400V/µs. The MAX4305, compensated for 10V/V or greater, delivers 350MHz and 1400V/µs.

MAX4104/MAX4105 and MAX4304/MAX4305 op amps are available in 5-pin SOT23 and 8-pin SO packages, with prices starting at $1.70 (1000 up, FOB USA).



NEW PRODUCTS

ICs feature 8MHz op amp, 185ns comparator, 10ppm reference in 8-pin µMAX

The MAX9000 series ICs perform high-speed signal detection. All contain an op amp and comparator; four contain a precision, 1.230V ±1% voltage reference as well. Each operates from a single supply of +2.5V to +5.5V and draws only 340µA of quiescent supply current. A shutdown mode that lowers the supply current to 2µA and places the outputs in a high-impedance state makes the MAX9001/MAX9004 devices ideal for portable applications.

Op amps in the MAX9000/MAX9001/MAX9002 ICs are compensated for unity-gain stability and exhibit gain-bandwidth products of 1.25MHz. MAX9003/MAX9004/MAX9005 op amps are stable for closed-loop gains of 10V/V or greater, and exhibit gain bandwidth products of 8MHz. The input common-mode ranges extend from 150mV below the negative rail to within 1.2V of the positive rail for the op amp (and to within 1.1V of the positive rail for the comparator).

The amplifier/comparator outputs can swing rail-to-rail, and they maintain excellent DC accuracy while delivering ±2.5mA for the amplifier and ±4.0mA for the comparator. Novel design in the comparator output stage eliminates power-supply glitches by substantially reducing the switching current during output transitions. The comparator's built-in ±2mV hysteresis provides noise immunity and prevents oscillation, even for slow-moving input signals.

The internal bandgap reference (MAX9000/MAX9001 and MAX9003/MAX9004) has a low temperature coefficient (8ppm/°C) and can sink or source as much as 1mA. (For MAX9000 and MAX9003 devices, the comparator's inverting input is internally connected to the reference output.) The op amp and reference outputs are stable with capacitive loads as high as 250pF and 100nF, respectively.

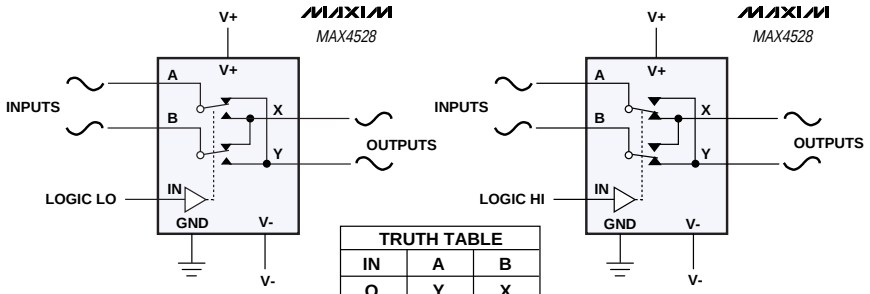
Package options include an 8-pin µMAX or 8-pin SO (MAX9000/MAX9002 and MAX9003/MAX9005), and a 10-pin µMAX or 14-pin SO (MAX9001/MAX9004). Prices start from $1.20 (1000 up, FOB USA).

Low-voltage analog phase-reversal switch handles rail-to-rail signals

The MAX4528 is a low-voltage CMOS analog IC configured as a phase-reversal switch (two SPDT types with internal connections). Fast transition times (100ns maximum with ±5V supplies), low charge injection (5pC maximum), and matched on-resistances (Δ4Ω maximum) optimize the device for high-speed applications such as synchronous (balanced) modulators and demodulators.

The MAX4528 operates on a single supply of +2.0V to +12V or a dual supply in the range ±2.7V to ±6V. Supply currents are 10µA maximum. The switches handle rail-to-rail analog signals and exhibit on-resistances of 70Ω (with ±5V supplies). Off-leakage currents are 10nA at +25°C and 100nA at +85°C.

The digital input includes protection against electrostatic discharge (ESD) as high as 2kV, and its logic thresholds (0.8V and 2.4V) ensure compatibility with TTL and CMOS logic signals. The MAX4528 is available in 8-pin µMAX, DIP, and SO packages. Prices start at $0.98 (1000 up, FOB USA).



TRUTH TABLE		
IN	A	B
0	Y	X
1	X	Y

Multiplexer/switch ICs offer low-voltage, single-supply operation

The MAX4524/MAX4525 CMOS analog switches are configured as a 4-channel multiplexer/demultiplexer (MAX4524) and a DPDT switch (MAX4525). They operate from a single supply of +2V to +12V, and are optimized for both 3V and 5V operation. On-resistance is 200Ω with a 5V supply and 500Ω with a 3V supply. All switches handle rail-to-rail analog signals, and both devices include inhibit inputs that open all signal paths simultaneously.

Off-leakage currents are only 2nA at +25ºC (20nA at +85ºC). Logic thresholds for the digital inputs (0.8V and 2.4V) ensure TTL/CMOS compatibility when operating with a 5V supply. MAX4524/MAX4525 devices are available in 10-pin µMAX packages, with prices starting at $1.10 (1000 up, FOB USA).

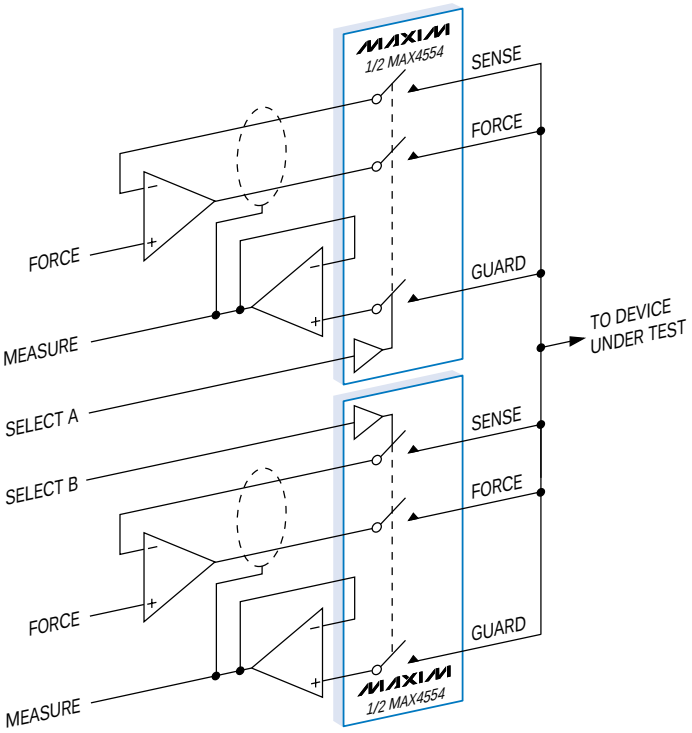
NEW PRODUCTS

Force-sense switches provide Kelvin sensing for ATE

The MAX4554/MAX4555/MAX4556 ICs are configured as force-sense analog switches for Kelvin sensing in automatic test equipment (ATE). Other applications include calibrators, precision power supplies, automatic calibration circuits, and asymmetric digital subscriber lines (ADSL) with loopback. Each device contains one or more high-current, low-resistance switches for forcing current, and two or more higher resistance switches for sensing voltage or switching guard signals.

Each device operates from a single supply in the +9V to +40V range, or dual supplies in the ±4.5V to ±20V range. Power consumption is only 1µW. For devices operating on ±15V supplies, the force-path on-resistances are 6Ω maximum, matched to within 1Ω. Sense-path on-resistances are 60Ω maximum, matched to within 8Ω. All switches handle rail-to-rail analog signals, and their off-leakage current is only 0.25nA at +25°C (2.5nA at +85°C). All digital inputs specify 0.8V/2.4V thresholds for TTL- and CMOS-logic compatibility. All devices feature >2kV ESD protection per MIL-STD-883, Method 3015.7.

The MAX4554 contains two force switches, two sense switches, and two guard switches configured as triple-pole/single-throw, normally open switches. The MAX4555 contains four independent SPST switches that are normally closed and the MAX4556 contains three SPDT switches, of which one is a force switch and two are sense switches. MAX4554/MAX4555/MAX4556 devices are available in 16-pin DIP, narrow SO, and QSOP packages. Prices start at $2.42 (1000 up, FOB USA).

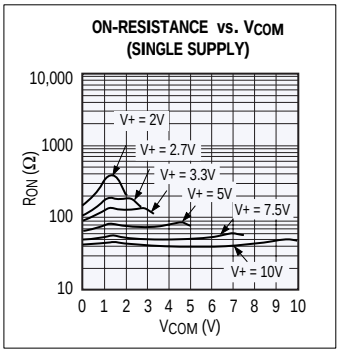


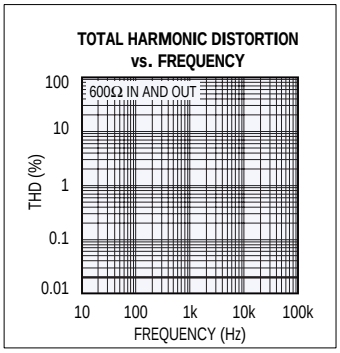
Low-voltage CMOS muxes and switches have 80Ω on-resistances

The MAX4581/MAX4582/MAX4583 series of CMOS analog ICs includes an 8-channel multiplexer (MAX4581), a dual 4-channel multiplexer (MAX4582), and a triple single-pole/double-throw switch (MAX4583). Each guarantees low on-resistance (80Ω) and continuous low-voltage operation (+2V to +12V with a single supply, and ±2V to ±6V with a dual supply).

MAX4581/MAX4582/MAX4583 devices are pin-compatible with industry-standard 74HC4051/74HC4052/74HC4053 devices. These parts handle rail-to-rail analog signals. They guarantee closely matched on-resistance between channels (4Ω maximum), and low on-leakage current: 1nA at +25°C and 5nA at +85°C. All digital inputs have standard logic thresholds (0.8V and 2.4V) that ensure compatibility with TTL/CMOS logic when operating with 5V or ±5V supplies.

MAX4581/MAX4582/MAX4583 devices are available in 16-pin QSOPs, DIPs, and narrow-SO packages. Prices start at $0.63 (1000 up, FOB USA).





NEW PRODUCTS

95% efficient DC-DC converters power RF PAs in wireless phones

MAX1700/MAX1701/MAX1703 step-up DC-DC converters generate the high current needed to drive RF power amplifiers in today's wireless telephones. Featuring an internal synchronous rectifier and power switch, these ICs achieve efficiencies as high as 95%. MAX1700/MAX1701 converters deliver output currents as high as 800mA, and reside in 16-pin QSOP packages that occupy the same board area as an 8-pin SO. The MAX1703 resides in a 16-pin narrow-SO package and delivers as much as 1.5A.

MAX1700/MAX1701/MAX1703 converters are designed to operate from batteries such as 1-to-3-cell NiCd/NiMH and 1-cell Li-Ion types. The converters run in bootstrap mode (powered by their own stepped-up output voltage), and are guaranteed to start from inputs as low as 1.1V. Once started, they maintain regulation for inputs as low as 0.7V. The output voltage can be preset to 3.3V or 5V, or adjusted from 2.5V to 5.5V using an external resistor-divider.

Pulse-width modulation and a constant high switching frequency of 300kHz minimize the converters' noise during full-power operation. To maximize battery life while providing up to 150mA for receiver and standby functions, a low-power mode lowers the quiescent current to 40µA (in shutdown, it drops to only 1µA).

The MAX1700 and MAX1701 feature dual shutdown controls that enable push-on/push-off operation with a single momentary switch. The MAX1701 and MAX1703 also include a comparator for generating a low-battery warning or power-good signal, and a gain block useful in building a low-dropout linear regulator for powering DSP, radio baseband, and other phone functions.

The MAX1700/MAX1701/MAX1703 are specified for the extended-industrial temperature range (-40°C to +85°C), with prices starting at $3.25 (1000 up, FOB USA). To help speed designs, Maxim offers complete evaluation kits and recommendations for the external components.

High-speed step-down controller for CPUs employs synchronous rectification

The MAX1639 is an ultra-high-performance, step-down DC-DC controller for generating CPU power in high-end computer systems. Designed for demanding applications in which output-voltage precision and good transient response are critical to proper operation, the MAX1639 operates from a 5V ±10% supply and delivers more than 35A from outputs that are ±1% accurate in the range 1.1V to 4.5V.

The MAX1639's excellent dynamic response prevents the output transients otherwise caused by the latest dynamically clocked CPUs. Its flying-capacitor bootstrap circuitry drives inexpensive, external n-channel MOSFETs, and synchronous rectification enables the controller to achieve efficiencies exceeding 90%. Users can pin-select a switching frequency of 300kHz, 600kHz, or 1MHz. Higher switching frequencies save board area and system cost through the use of a smaller surface-mount inductor and output-filter capacitor.

To protect the output against overvoltage, a crowbar circuit turns on the low-side MOSFET (with 100% duty factor) when the output rises 200mV above the normal regulation point. Other features include an internal digital soft-start, power-good output, and 3.5V ±1% reference output. The MAX1639 is available in a 16-pin narrow-SO package specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $3.39 (1000 up, FOB USA).

Serial-parallel load-switch controllers have SMBus interface

MAX1661/MAX1662/MAX1663 load-switch controllers are designed to control external power MOSFETs. Mounted on a system motherboard, the small, low-cost devices control point-of-load switching from a 2-wire SMBus™ serial interface. Each device has three bidirectional terminals that are capable of serving either as TTL-compatible logic inputs or as high-voltage, open-drain outputs.

The bidirectional pins withstand 28V, enabling them to control the battery-voltage distribution switches in a notebook computer. In addition, their input capability enables the use of MAX1661/MAX1662/MAX1663 devices in serial-to-parallel and parallel-to-serial applications: either routing serial-input data to the three parallel outputs, or accepting digital data at those outputs and formatting it for transmission via the serial SMBus.

MAX1661 outputs are intended for driving n-channel MOSFETs, so they are active-low at power-up. MAX1662/MAX1663 outputs are intended for driving p-channel MOSFETs, so they assume a high-impedance state at power-up. These conditions enable the ICs to perform power-plane sequencing by ensuring that the MOSFETs are off at power-up.

Operating on a single supply of 2.7V to 5.5V, the MAX1661/MAX1662/MAX1663 draw only 3µA of supply current. To eliminate latencies introduced by the serial bus, their SMBSUS inputs select between two internal control-data registers, enabling the host system to select between two different power-plane configurations. Other features include thermal-overload and overcurrent protection, ultra-low supply current, and hardware/software interrupt capabilities.

An evaluation kit (MAX1662EVKIT) is available to aid evaluations and speed the design cycle. The MAX1661/MAX1662/MAX1663 are available in space-saving µMAX packages. Prices start at $1.29 (1000 up, FOB USA).

SMBus is a trademark of Intel Corp.

NEW PRODUCTS

Digitally adjustable DC-DC converter provides ±28V for LCDs and varactors

The MAX686 is a high-efficiency boost converter that generates a positive or negative high voltage from a low-voltage input. Its internal 6-bit D/A converter provides a digitally adjustable bias voltage for the LCD in a handheld instrument or for the varactor tuner in a set-top box. To save space and cost, the required power switch is included on-chip. The device's internal DAC, low supply current, small package, and tiny external components provide an extremely compact and efficient high-voltage supply for LCDs.

A polarity-select pin enables the MAX686 to generate either a positive or negative output voltage. The IC requires a supply voltage of +2.7V to +5.0V, but the step-up inductor can operate directly from a battery or from any voltage between 0.8V and V_{OUT}. The MAX686 can deliver 10mA at +28V or -28V.

To achieve efficiencies up to 93% over a wide range of load conditions, the MAX686 employs a current-limited pulse-frequency-modulation (PFM) control scheme. Its low operating current (70µA) drops to 1µA in shutdown mode, making the MAX686 ideal for use in battery-powered applications. High switching frequency (to 300kHz) and a pin-selectable current limit of 500mA or 250mA enables the use of tiny, inexpensive inductors.

The MAX686 is available in a 16-pin QSOP package—the same size as an 8-pin SO. Prices start at $2.95 (1000 up, FOB USA).

Converters boost 3V to 5V at 250mA without inductors

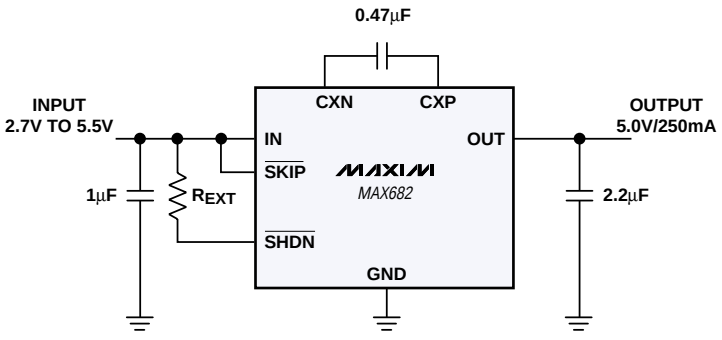
MAX682/MAX683/MAX684 step-up DC-DC converters challenge the use of inductor-based DC-DC converters while setting new performance standards for charge pumps: accepting inputs in the range 2.7V to 5.5V, they generate regulated 5V outputs with maximum output currents of 250mA, 100mA, and 50mA respectively.

The MAX682/MAX683/MAX684 are high-efficiency, local power supplies that provide 5V from a 3.3V input in compact applications. They require one resistor, three small capacitors, and no inductors. In shutdown mode they draw only 0.1µA. The converters' high switching frequency and unique regulation scheme allow the use of output capacitors as small as 1µF per 100mA of output current.

Regulation is achieved either by skip mode or by constant-frequency (linear) mode. In skip mode the converters vary the switching frequency as a function of load current, producing On-Demand™ switching that results in very small external capacitors and very low quiescent supply current. For heavy loads, they transfer energy from input to output at frequencies to 2MHz. For light loads, they switch more slowly, limiting the quiescent supply current to only 100µA.

In constant-frequency mode the switching rate is constant at all load currents, with regulation accomplished by controlling the switching-path resistance. This technique provides a constant-frequency ripple that is easily filtered for low-noise applications. An external resistor sets the constant frequency between 50kHz and 2MHz.

The 250mA MAX682 is available in an 8-pin SO package. The 100mA MAX683 and 50mA MAX684 are available in space-saving 8-pin µMAX packages only 1.1mm high. Prices for the MAX684 start at $1.65 (1000 up, FOB USA).



Regulated negative supply delivers 125mA without inductors

The MAX1673 DC-DC converter is an inverting charge pump that accepts positive input voltages in the 2V to 5.5V range and generates a regulated negative output voltage as high as $-V_{IN}$. It delivers output currents up to 125mA. Two external resistors set the output voltage, and three small external capacitors support the charge pump.

The MAX1673 regulates by skip mode or by linear mode. In skip mode, it varies the switching frequency according to load current. This On-Demand™ switching permits very small capacitors and very low quiescent supply current. For heavy loads, the converter transfers energy from input to output at 350kHz. For light loads, it switches more slowly, limiting the quiescent supply current to 35µA.

In linear mode, the MAX1673 switches at a constant 350kHz regardless of load current, and regulates by controlling the switching-path resistance. This technique provides a constant-frequency ripple that is easily filtered for low-noise applications. The MAX1673 also includes a 1µA logic-controlled shutdown mode.

The MAX1673 is available in an 8-pin SO package specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $1.95 (1000 up, FOB USA).

On-Demand is a trademark of Maxim Integrated Products.

NEW PRODUCTS

µP supervisors offer 3,224 unique monitoring combinations

The MAX6316–MAX6322 family of microprocessor (µP) supervisory circuits are designed for monitoring the power-supply voltages and µP activity in digital systems. They offer a software watchdog, manual reset, and several combinations of push/pull, open-drain, and bidirectional (Motorola 68HC11-compatible) reset outputs. For a listing of functions associated with each of the ten devices, see Maxim's *Product Selector Guide*.

The available product variations include 26 factory-trimmed reset voltages (in increments of 100mV from 2.5V to 5V), one of four minimum reset-timeout periods (1ms, 20ms, 140ms, or 1.12sec), and one of four minimum watchdog-timeout periods (6.3ms, 102ms, 1.6sec, or 25.6sec). The products draw supply currents as low as 5µA, and each is designed to ignore fast negative transients on V_{CC}. The reset outputs are guaranteed valid for V_{CC} down to 1V.

MAX6316–MAX6322 devices are available in 5-pin SOT23 packages specified for the commercial temperature range (0°C to +70°C), with prices starting at $1.14 (2500 up, FOB USA). The minimum order for nonstandard versions is 10,000 pieces. Contact the factory for availability.

**MAX6317/MAX6321/MAX6322 are future products—contact factory for availability.*

1µA, 1Mbps, 3V RS-232 ICs for portable applications meet ±15kV ESD standards

The MAX3224E–MAX3227E ICs are high-speed, low-power, 3V RS-232 devices for use in portable and battery-powered products that require compliance with international standards for immunity to electrostatic discharge (ESD). All transmitter outputs and receiver inputs are protected to ±15kV using the Human Body Model or the IEC 1000-4-2 Air-Gap Discharge method, and to ±8kV using the IEC 1000-4-2 Contact-Discharge model.

The MAX3224E and MAX3225E each contain two transmitters and two receivers, and (for size-constrained applications that do not require extra handshaking or control lines) the MAX3226E and MAX3227E each contain one transmitter and one receiver in a 16-pin SSOP package. Low supply current (1µA) maximizes the battery life for each device. The MAX3224E/MAX3226E guarantee data rates to 250kbps, and the MAX3225E/MAX3227E (which include Maxim's MegaBaud™ feature) guarantee 1Mbps for high-speed applications such as ISDN-modem communications.

A proprietary voltage doubler and an output stage with low dropout voltage allow the MAX3224E–MAX3227E to deliver true RS-232 performance over the V_{CC} range 3V to 5.5V. Unlike power-hungry voltage triplers, these devices require only four external capacitors regardless of the supply voltage. Maxim's AutoShutdown Plus™ architecture enables automatic power savings without changes to software.

After 30 seconds with no valid RS-232 activity (as, for example, when the RS-232 cable is disconnected or when the device is not actively communicating with a connected peripheral), the MAX3224E–MAX3227E enter a low-power shutdown mode. They exit shutdown on detecting valid activity at any receiver or transmitter input. The RS-232 receivers are always active, even in shutdown mode.

Available package options include DIPs and SSOPs. Prices start from $2.24 for the MAX3224E/MAX3225E and from $1.45 for the MAX3226E/MAX3227E (1000 up, FOB USA).

MegaBaud is a trademark of Maxim Integrated Products.

AutoShutdown Plus is a trademark of Maxim Integrated Products.

10Mbps, 3V/5V quad RS-422 receivers feature ±15kV ESD protection

The MAX3095/MAX3096 quad RS-422 receivers include protection against electrostatic discharge (ESD) for compliance with international standards. The first such products to offer ±15kV ratings, they provide robust, internal ESD protection tested to stringent, industry-recognized standards. All receiver inputs are ESD-protected to ±15kV using the Human Body model and the IEC 1000-4-2 Air-Gap Discharge method, and to ±8kV using the IEC 1000-4-2 Contact Discharge method.

The MAX3095 operates from a +5V supply, and the MAX3096 operates from a +3.3V supply. Receiver propagation delays are guaranteed to within ±8ns of a predetermined value, thereby ensuring a maximum skew of 16ns between devices—even between devices from different production lots. This performance is ideal for bus receivers in telecommunications equipment.

Operating at data rates to 10Mbps, the MAX3095 and MAX3096 feature a quarter-unit-load input impedance that allows 128 receivers on a bus. Complementary-enable inputs can place either device in a low-power shutdown mode, in which the receiver outputs are high impedance and the supply current drops to 1nA. Operating supply current is only 2.4mA.

Both devices are pin-compatible with the industry-standard '26LS32. They come in space-saving 16-pin QSOP packages as well as 16-pin DIP and narrow-SO packages, with prices starting at $2.02 (1000 up, FOB USA).

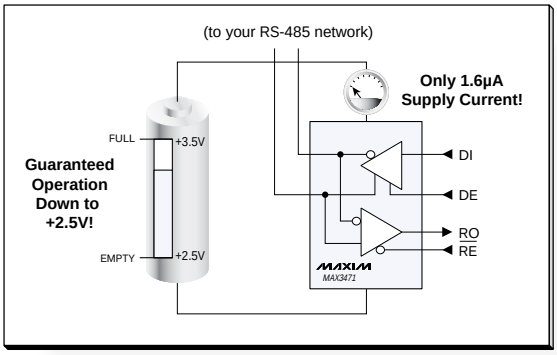
NEW PRODUCTS

Differential RS-485/ RS-422 transceiver draws only 1.6µA

The MAX3471 is a half-duplex data transceiver intended for battery-powered RS-485/RS-422 applications. It draws only 1.6µA (typical) from a +3.6V supply and its wide range of supply voltage (+2.5V to +5.5V) guarantees operation over the lifetime of a lithium battery.

True fail-safe operation guarantees a logic-high receiver output when the receiver inputs are open or shorted. Thus, the MAX3471 receiver output goes high when all transmitters on a terminated bus are disabled and high impedance. Internal circuitry prevents battery back-charging when the MAX3471 driver outputs are enabled and pulled above V_{CC} or below ground. The MAX3471 input resistance is equivalent to a 1/8 unit load.

The MAX3471 is available in an 8-pin µMAX package, with prices starting at $1.69 (1000 up, FOB USA).



Low-power IF transceiver includes limiter, RSSI, and quad modulator

The MAX2510 intermediate-frequency (IF) transceiver incorporates a multitude of functions in an ultra-small package. Its design suits two major application groups: those with a first IF of 200MHz to 500MHz and a second IF up to 30MHz, and those with an RF input of 200MHz to 500MHz and a first IF up to 30MHz. They include PCS systems such as PWT1900, PACS, PHS, and DECT phones and base stations, 400MHz ISM transceivers, IF transceivers, and wireless data links.

The MAX2510 receiver section consists of a downconverter mixer and limiting amplifier with RSSI. The mixer has excellent dynamic range. Its input 1dB compression point is -23dBm, making it ideal for applications in which considerable interference is expected (PCS systems in the U.S., for example). The received-signal-strength indicator (RSSI), derived from the limiting amplifier, has more than 90dB of dynamic range and excellent linearity. Its guaranteed maximum relative error is ±2dB.

The transmitter section includes a quadrature modulator with excellent sideband suppression (40dB), followed by a variable-gain, 0dBm output-buffer amplifier. To extend battery life, the amplifier's unique biasing scheme adjusts current draw to the minimum necessary for sustaining the desired level of output power.

The MAX2510's range of operating supply voltage (+2.7V to +5.5V) enables direct connection to a 3-cell battery. A shutdown mode lowers the chip's supply current below 2µA.

As an alternative for applications that require image rejection at the receiver as well as the transmitter, the MAX2511 includes all features found in the MAX2510 (limiter, RSSI, control functions, etc.). The MAX2510 comes in a 28-pin QSOP, with prices starting at $5.35 (1000 up, FOB USA).

Low-cost RF up/downconverters include LNA and PA driver

The MAX2410 and MAX2411A are low-cost silicon-bipolar up/down-converters. Each performs transmit and receive functions for the RF front-end in time-division-duplex (TDD) communication systems. The MAX2410/MAX2411A operate over a wide frequency range and are optimized for RF frequencies around 1.9GHz. Applications include most of the popular cordless and PCS standards: PWT1900/DCT1900, PHS, and DECT.

The MAX2410 includes a low-noise amplifier with 2.4dB noise figure and -10dBm input 3rd-order intercept point (IIP3), a downconverter mixer with a low 9.8dB noise figure and 3.3dBm IIP3, an upconverter mixer, a local oscillator buffer, and a variable-gain PA driver amplifier. This amplifier's gain is user-adjustable through an applied analog voltage, with a maximum of 15dB and a minimum of -20dB (typical).

The MAX2410 has separate IF ports for receive and transmit. The MAX2411A offers the same functionality as the MAX2410, but its unique, bidirectional, differential IF port reduces cost and component count by allowing the transmit and receive paths to share the same IF filter. Both devices feature flexible power-down modes and low power consumption: 60mW in receive, 90mW in full-power transmit, and only 0.3mW in shutdown mode.

MAX2410/MAX2411A devices are available in 28-pin QSOPs specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $3.47 (1000 up, FOB USA).

NEW PRODUCTS

3-in-1 silicon delay line has ±2ns accuracy

The MXD1013 is a monolithic IC containing three independent delay lines with logic buffers. Internal compensation maintains the nominal delay value over specified ranges of temperature and supply voltage. Nominal specified accuracy applies to the leading or trailing edge: ±2ns from 10ns to 60ns, ±3% from 70ns to 100ns, and ±5% from 150ns to 200ns.

Nominal delay values come in 18 discrete levels from 10ns to 200ns, as indicated by a 3-digit suffix on the part number (consult the factory for custom values). Each output can drive as many as ten standard 74LS loads. The MXD1013 draws 20mA of supply current, versus 40mA for the DS1013 from Dallas Semiconductor. When compared with hybrid devices, the MXD1013 offers better performance, higher reliability, and lower cost.

Package options for the MXD1013 include a space-saving 8-pin µMAX package, an 8-pin SO or plastic DIP, a 14-pin plastic DIP, and a 16-pin narrow SO. Prices start at $2.73 (1000 up, FOB USA).

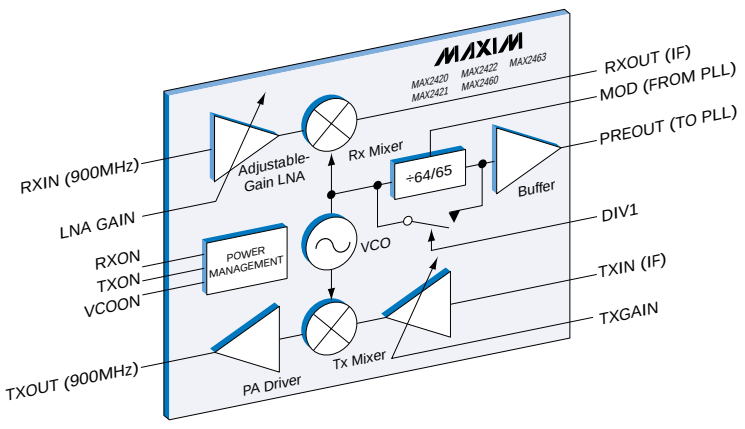
Image-reject RF ICs suit low-cost 900MHz radios

Highly integrated RF-transceiver ICs in the MAX242X/MAX246X series and RF-receiver ICs in the MAX244X series reduce the cost of 900MHz cordless telephones, wireless modems, and RF transceivers. Unlike conventional RFICs, these devices include active image-reject mixers that reduce cost and space by eliminating the need for external RF filters. For further savings in cost and space, the majority of these devices are optimized for a low receive-IF frequency that eliminates the need for additional frequency-conversion stages.

Typical receive and transmit image rejection is 35dB. The front-end LNA's 1.8dB noise figure allows for a combined downconverter noise figure of just 4dB. Adjustable gain in the LNA lets users increase the receiver's dynamic range, from an IIP3 of -17dBm at maximum LNA gain to +2dBm IIP3 at minimum LNA gain. Phase noise in the internal VCO is just -84dBc/Hz at 10kHz offset. The built-in prescaler can operate either in divide-by-64/65 mode with a CMOS PLL or in buffer mode with a BiCMOS synthesizer.

MAX2420/MAX2421/MAX2422 and MAX2460/MAX2463 ICs, with image-reject capability in the transmit and receive paths, are optimized for IFs between 10.7MHz and 110MHz. MAX2424/MAX2426 ICs, which replace the transmit image-reject mixer with a double-balanced mixer, are compatible with BPSK modulation and with applications that modulate the VCO directly. MAX2440–MAX2442 ICs are receive-only devices.

The ten ICs of the MAX242X/MAX244X/MAX246X family operate from a single supply of +2.7V to +4.8V, allowing direct connection to a 3-cell battery. Typical low supply currents are 23mA for the receiver, 26mA for the transmitter, and 9.5mA for the oscillator. Current draw in the shutdown mode is only 0.5µA. The devices come in 28-pin SSOP packages, with prices starting at $2.98 (1000 up, FOB USA).



Upstream CATV driver amp has programmable gain

The MAX3532 is a programmable power amplifier designed for use in upstream cable applications. Driven with a 36dBmV continuous-wave input and driving a 1:2 (voltage ratio) transformer, the MAX3532 generates an output of 62dBmV maximum. Gain is variable in 1dB steps from 0dBmV to 62dBmV, controlled via a 3-wire serial digital bus. The operating frequency range is 5MHz to 42MHz.

The MAX3532 has three modes of operation: high-power mode offers the maximum output power; low-noise mode generates minimum noise at lower power levels; and transmit disable mode—for use between bursts in TDMA systems—provides minimum output noise with high isolation. The device operates on a single +5V supply and consumes 350mW (typical).

Two power-down modes are available. Software shutdown mode powers down all analog circuitry while maintaining the programmed gain setting, and hardware shutdown mode lowers the supply current below 50µA by disabling all internal circuitry. The MAX3532 is available in a 36-pin SSOP, with prices starting at $4.45 (1000 up, FOB USA).